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## NOTICE OF ALLOWANCE AND FEE(S) DUE

54975 7590 12/29/2009

HOLLAND & KNIGHT LLP  
10 ST. JAMES AVENUE  
BOSTON, MA 02116-3889

EXAMINER

SWEARINGEN, JEFFREY R

ART UNIT

PAPER NUMBER

2445

DATE MAILED: 12/29/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/069,670

02/22/2002

Xavier Leroy

102114.00034

3622

TITLE OF INVENTION: MANAGEMENT PROTOCOL, METHOD FOR VERIFYING AND TRANSFORMING A DOWNLOADED PROGRAMME  
FRAGMENT AND CORRESPONDING SYSTEMS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$0	\$0	\$1510	03/29/2010

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.**

**THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.**

### HOW TO REPLY TO THIS NOTICE:

#### I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.**

# **PART B - FEE(S) TRANSMITTAL**

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE  
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

54975 7590 12/29/2009

**HOLLAND & KNIGHT LLP**  
10 ST. JAMES AVENUE  
BOSTON, MA 02116-3889

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## **Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/069,670 02/22/2002 Xavier Leroy 102114.00034 3622

TITLE OF INVENTION: MANAGEMENT PROTOCOL, METHOD FOR VERIYING AND TRANSFORMING A DOWNLOADED PROGRAMME  
FRAGMENT AND CORRESPONDING SYSTEMS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional NO \$1510 \$0 \$0 \$1510 03/29/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
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SWEARINGEN, JEFFREY R 2445 709-220000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 \_\_\_\_\_
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 \_\_\_\_\_
- 3 \_\_\_\_\_

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies \_\_\_\_\_

4b. Payment of Fee(s); (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number \_\_\_\_\_ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature \_\_\_\_\_

Date \_\_\_\_\_

Typed or printed name \_\_\_\_\_

Registration No. \_\_\_\_\_

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/069,670	02/22/2002	Xavier Leroy	102114.00034	3622
54975	7590	12/29/2009	EXAMINER	
HOLLAND & KNIGHT LLP 10 ST. JAMES AVENUE BOSTON, MA 02116-3889			SWEARINGEN, JEFFREY R	
			ART UNIT	PAPER NUMBER
			2445	
DATE MAILED: 12/29/2009				

## Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

<b>Notice of Allowability</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/069,670	LEROY, XAVIER	
	<b>Examiner</b>	<b>Art Unit</b>	
	Jeffrey R. Swearingen	2445	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to telephonic conversation of 12/14/09 and amendments of 9/28/09.
2. ☒ The allowed claim(s) is/are 4-6,8-14,20,22 and 24-28.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☒ All    b) ☐ Some\*    c) ☐ None    of the:
    1. ☒ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
  - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
    - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_.
  - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_.

**Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

- |  |   |
|--|---|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892)   | 5. <input type="checkbox"/> Notice of Informal Patent Application                     |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 6. <input type="checkbox"/> Interview Summary (PTO-413),<br>Paper No./Mail Date ____. |
| 3. <input checked="" type="checkbox"/> Information Disclosure Statements (PTO/SB/08),<br>Paper No./Mail Date <u>20090908</u> | 7. <input checked="" type="checkbox"/> Examiner's Amendment/Comment                   |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit<br>of Biological Material                   | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance  |
|  | 9. <input type="checkbox"/> Other ____.   |

/Rupal D. Dharia/  
Supervisory Patent Examiner, Art Unit 2400

### **EXAMINER'S AMENDMENT**

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Seth Milman on 12/14/2009.

The application has been amended as follows:

Claim 4. (Currently Amended) A method of verifying a program fragment downloaded onto a reprogrammable embedded system, equipped with a rewritable memory, a microprocessor and a virtual machine equipped with an execution stack and with operand registers, said program fragment consisting of an object code and including at least one subprogram consisting of a series of instructions manipulating said operand registers, said microprocessor and virtual machine configured to interpret said object code, said embedded system being interconnected to a reader, wherein subsequent to a detection of a downloading command and a storage of said object code in said rewritable memory, said method, for each subprogram, comprises:

initializing a type stack and a table of register types through data representing a state of said virtual machine on initialization of an execution of said temporarily stored object code;

carrying out a verification process of said temporarily stored object code instruction by instruction, by discerning an existence, for each current instruction, of a

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target, a branching-instruction target, a target of an exception-handler call or a target of a subroutine call, and, said current instruction being a target of a branching instruction, said verification process including verifying that said type stack is empty and rejecting said program fragment otherwise;

verifying and updating an effect of said current instruction on the data types of said type stack and of said table of register types including:

verifying that said type stack includes at least as many entries as said current instruction includes operands;

unstacking and verifying that types of entries at the top of said stack are subtypes of the types of said operands of said current instruction; and

stacking data types which are assigned to said results on said stack;

said verification process being successful when said table of register types is not modified in the course of a verification of all said instructions, and said verification process being carried out instruction by instruction until said table of register types is stable, with no modification having taken place, said verification process being interrupted and said program fragment being rejected, otherwise.

Claim 12. (Currently Amended) The method of claim 4, wherein said verifying and updating includes, ~~at least:~~

~~verifying that said type stack includes at least as many entries as said current instruction includes operands;~~

~~unstacking and verifying that types of entries at the top of said stack are subtypes of the types of said operands of said current instruction;~~

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verifying an existence of a sufficient memory space on said type stack to proceed to stack the results of said current instruction;

~~stacking data types which are assigned to said results on said stack.~~

Claim 20. (Currently Amended) An embedded system which can be reprogrammed by downloading program fragments, said embedded system including at least one microprocessor, one random-access memory, one input/output module, one electrically reprogrammable nonvolatile memory and one permanent memory, an installed main program and a virtual machine adapted to execute said installed main program and at least one program fragment using said microprocessor, wherein said embedded system includes at least one verification program module to verify a downloaded program fragment in accordance with a process comprising:

initializing a type stack and a table of register types through data representing a state of said virtual machine at a starting of an execution of said temporarily stored object code;

carrying out a verification process of said temporarily stored object code instruction by instruction, by discerning an existence, for each current instruction, of a target, a branching-instruction target, a target of an exception-handler call or a target of a subroutine call, and, said current instruction being a target of a branching instruction, said verification process including verifying that said type stack is empty and rejecting said program fragment otherwise;

carrying out a verification process and updating of an effect of said current instruction on the data types of said type stack and of said table of register types;

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verifying and updating an effect of said current instruction on the data types of said type stack and of said table of register types including:

verifying that said type stack includes at least as many entries as said current instruction includes operands;

unstacking and verifying that types of entries at the top of said stack are subtypes of the types of said operands of said current instruction; and

stacking data types which are assigned to said results on said stack;

said verification process being successful when said table of register types is not modified in the course of a verification of all of said instructions, and said verification process being carried out instruction by instruction until said table of register types is stable, with no modification having taken place, said verification process being interrupted and said program fragment being rejected, otherwise;

said verification program module being installed in said permanent memory.

Claim 22. (Currently Amended) A system for transforming an object code of a program fragment including a series of instructions, in which operands of each instruction belong to data types manipulated by said instruction, an execution stack does not exhibit any overflow phenomenon and for each branching instruction, the types of stack variables at said branching are identical to the types of stack variables at targets of this branching, and an operand, of given type, written to a register by an instruction of said object code is reread from the same register by another instruction of said object code with the same given data type, into a standardized object code for said program fragment, wherein said transforming system includes, at least, installed in a



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memory of a development computer or workstation, a program module for transforming said object code into a standardized object code in accordance with a process of transforming including for all instructions of said object code comprising:

annotating each current instruction with the data type of said type stack before and after execution of said current instruction, with an annotation data being calculated by means of analysis of the data stream relating to said current instruction;

detecting, within said instructions and within each current instruction, an existence of branchings, or respectively of branching-targets, for which said execution stack is not empty, said detecting operation being carried out on the basis of said annotation data of said type of stack variables allocated to each current instruction; and, in case of detection of a non-empty execution stack,

inserting instructions to transfer stack variables on either side of each said branching or branching target respectively, in order to empty contents of said execution stack into temporary registers before said branching and to reestablish said execution stack from said temporary registers after said branching; ~~and~~

not inserting any transfer instruction otherwise, this method allowing thus to obtain said standardized object code for said program fragment, in which said operands of each instruction belong to the data types manipulated by said instruction, said execution stack does not exhibit any overflow phenomenon, said execution stack is empty at each branching instruction and at each branching-target instruction, in the absence of any modification to the execution of said program fragment; and

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verifying and updating an effect of said current instruction on the data types of said type stack including:

verifying that said type stack includes at least as many entries as said current instruction includes operands;

unstacking and verifying that types of entries at the top of said stack are subtypes of the types of said operands of said current instruction; and

stacking data types which are assigned to said results on said stack; and

carrying out a verification process, said verification process being successful when a table of register types is not modified in the course of a verification of all said instructions, and said verification process being carried out instruction by instruction until said table of register types is stable, with no modification having taken place, said verification process being interrupted and said program fragment being rejected, otherwise.

Claim 24. (Currently Amended) A computer program product which is recorded on a computer readable storage medium and can be loaded directly from a terminal into an internal memory of a reprogrammable embedded system equipped with a microprocessor and a rewritable memory, said embedded system making it possible to download and temporarily store a program fragment consisting of an object code including a series of instructions, executable by said microprocessor by way of a virtual machine equipped with an execution stack and with operand registers manipulated via said instructions and making it possible to interpret said object code, said computer program product including portions of object code to execute at least one of steps of

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verifying a program fragment downloaded onto said embedded system according to a verifying process, said verifying process comprising:

initializing a type stack and a table of register types through data representing a state of said virtual machine at initialization of execution of said temporarily stored object code;

carrying out a verification process of said temporarily stored object code instruction by instruction, by discerning an existence, for each current instruction, of a target, a branching-instruction target, a target of an exception-handler call or a target of a subroutine call, and, said current instruction being a target of a branching instruction, said verification process consisting in verifying that said execution stack is empty and rejecting said program fragment otherwise;

carrying out a verification process and an updating of an effect of said current instruction on the data types of said type stack and of said table of register types; and

verifying and updating an effect of said current instruction on the data types of said type stack and of said table of register types including:

verifying that said type stack includes at least as many entries as said current instruction includes operands;

unstacking and verifying that types of entries at the top of said stack are subtypes of the types of said operands of said current instruction; and

stacking data types which are assigned to said results on said stack;

said verification process being successful when said table of register types is not modified in the course of a verification of all said instructions, and said verification

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process being carried out instruction by instruction until said table of register types is stable, with no modification having taken place, said verification process being interrupted and said program fragment being rejected, otherwise.

Claim 25. (Currently Amended) A computer program product which is recorded on a computer readable storage medium including portions of object code to execute steps of a process of transforming an object code of a downloaded program fragment into a standardized object code for said program fragment said process of transforming comprising:

annotating each instruction with a data type of a stack before and after execution of said current instruction, with said annotation data being calculated by means of an analysis of a data stream relating to said current instruction;

detecting, within said instructions and within each current instruction, an existence of branchings, or respectively of branching `[[ - ]]` targets, for which an execution stack is not empty, said detecting operation being carried out ~~on~~ based on said annotation data of a type of stack variables allocated to each current instruction, and, in case of detection of a non-empty execution stack `[[ ; ]]` :

inserting instructions to transfer stack variables on either side of each said branching or branching target respectively, in order to empty contents of said execution stack into temporary registers before said branching and to reestablish the execution stack from said temporary registers after said branching; ~~and~~

not inserting any transfer instruction otherwise, this method allowing thus:

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to obtain said standardized object code for said program fragment, in which the operands of each instruction belong to the data types manipulated by said instruction, said execution stack does not exhibit any overflow phenomenon, said execution stack is empty at each branching instruction and at each branching-target instruction, in absence of any modification to an execution of said program fragment; and

to verify any update an effect of said current instruction on a data type of a type stack including:

verifying that said type stack includes at least as many entries as said current instruction includes operands;

unstacking and verifying that types of entries at the top of said stack are subtypes of the types of said operands of said current instruction;

stacking data types which are assigned to said results on said stack; and

to carry out a verification process, said verification process being successful when a table fo register types is not modified in the course of a verification of all said instructions, and said verification process being carried out instruction by instruction until said table of register types is stable, with no modification having taken place, said verification process being interrupted and said program fragment being rejected, otherwise.

Claim 26. (Currently Amended) A computer program product which is recorded on a computer readable storage medium and can be used in a reprogrammable embedded system, equipped with a microprocessor and a rewritable memory, said reprogrammable embedded system allowing to download a program fragment consisting of an object code, a series of instructions, executable by said microprocessor of said reprogrammable embedded system by means of a virtual machine equipped with an execution stack and with local variables or registers manipulated via instructions and making it possible to interpret said object code, said computer program product comprising:

program resources which can be read by said microprocessor of said embedded system via said virtual machine, to command execution of a procedure for managing a downloading of a downloaded program fragment;

program resources which can be read by said microprocessor of said embedded system via said virtual machine, to command execution of a procedure for verifying, by instruction, said object code which makes up said program fragment including:

program resources for verifying and updating an effect of said instruction on a data type of a type stack and of a table of register types including:

verifying that said type stack includes at least as many entries as said current instruction includes operands;

unstacking and verifying that types of entries at the top of said type stack are subtypes of the types of said operands of said current instruction; and

stacking data types which are assigned to said results on said stack; and

program resources for carrying out a verification process, said verification process being successful when said table of register types is not modified in the course of a verification of all said instructions, and said verification process being carried out instruction by instruction until said table of register types is stable, with no modification having taken place, said verification process being interrupted and said program fragment being rejected, otherwise:

program resources which can be read by said microprocessor of said embedded system via said virtual machine, to command execution of a downloaded program fragment subsequent to or in the absence of a conversion of said object code of said program fragment into a standardized object code for this same program fragment.

The following is an examiner's statement of reasons for allowance: Applicant's added elements to the independent claims involving the verification elements of "verifying and updating an effect of said current instruction on the data types of said type stack and of said table of register types including: verifying that said type stack includes at least as many entries as said current instruction includes operands; unstacking and verifying that types of entries at the top of said stack are subtypes of the types of said operands of said current instruction; and stacking data types which are assigned to said results on said stack; said verification process being successful when said table of register types is not modified in the course of a verification of all said

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instructions, and said verification process being carried out instruction by instruction until said table of register types is stable, with no modification having taken place, said verification process being interrupted and said program fragment being rejected, otherwise" are not taught in the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. Swearingen whose telephone number is (571)272-3921. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivek Srivastava can be reached on 571-272-7304. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



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Jeffrey R. Swearingen  
Examiner  
Art Unit 2445

/J. R. S./  
Examiner, Art Unit 2445

/Rupal D. Dharia/  
Supervisory Patent Examiner, Art Unit 2400